

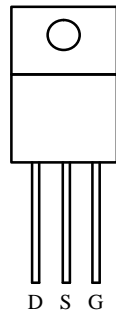
**N-Channel Enhancement-Mode Transistors**

**Product Summary**

$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
100	0.081	34

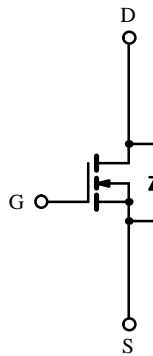
Parametric limits in accordance with MIL-S-19500/592 where applicable.

**TO-254AA  
Hermetic Package**



Top View

Case Isolated



N-Channel MOSFET

**Absolute Maximum Ratings ( $T_C = 25^\circ\text{C}$  Unless Otherwise Noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current	$I_{DM}$	136	
Avalanche Current	$I_{AR}$	34	
Maximum Power Dissipation	$P_D$	150	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

**Thermal Resistance Ratings**

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Case	$R_{thJC}$	0.83	$^\circ\text{C/W}$

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1493.

## Specifications ( $T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ <sup>a</sup>	Max	
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1000\ \mu\text{A}$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}, T_J = -55^\circ\text{C}$			5.0	
		$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}, T_J = 25^\circ\text{C}$	2.0		4.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}, T_J = 125^\circ\text{C}$			$\pm 200$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			25	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			250	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			1000	
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 34\text{ A}$			0.081	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 21\text{ A}, T_J = 125^\circ\text{C}$			0.11	
<b>Dynamic</b>						
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 34\text{ A}$	50		125	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$		8		22	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$		15		65	
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 1.47\ \Omega$ $I_D \cong 34\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.35\ \Omega$			35	ns
Rise Time <sup>c</sup>	$t_r$				190	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$				170	
Fall Time <sup>c</sup>	$t_f$				130	
<b>Source-Drain Diode Ratings and Characteristics</b>						
Continuous Current	$I_S$				34	A
Pulsed Current	$I_{SM}$				136	
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_F = 34\text{ A}, V_{GS} = 0\text{ V}$			1.8	V
Reverse Recovery Time	$t_{rr}$	$I_F = 34\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$			500	ns

Notes:

- For design aid only; not subject to production testing.
- Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Independent of operating temperature.